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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/800,851	03/07/2001	John F. Hutton	10006513-1	5597

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EXAMINER	
WANG, ALBERT C	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/800,851	HUTTON ET AL.	
	Examiner	Art Unit	
	Albert Wang	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24 and 26-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24 and 26-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is responsive to the amendment filed January 14, 2005.

2. The declaration filed on January 14, 2005 under 37 CFR 1.131 is sufficient to overcome the Stinson reference.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 10, 21, 23, 24, 26 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Hatzilambrou et al., "Ring Oscillator Sensitivity to Spatial Process Variation", Presented: 1st International Workshop on Statistical Metrology, June 1996 ("Hatzilambrou").

As per claim 1, Hatzilambrou discloses a method for detecting process variations, the method comprising:

controlling count gate control by a first circuit (fig. 2, by mux; sec. 2);

generating at least one clock count by a second circuit (fig. 2, by ring oscillator RO1; sec. 2); and

outputting results of the clock count by a third circuit (fig. 2, by count/shift register; sec. 2).

As per claim 10, Hatzilambrou discloses an apparatus to detect process variations comprising:

a first circuit to select a clock (fig. 2, mux; sec. 2);

a second circuit connected to the first circuit to generate at least one clock count (fig. 2, ring oscillator RO1; sec. 2); and

a third circuit connected to the first circuit to output a result of the clock count (fig. 2, count/shift register; sec. 2).

As per claim 21, Hatzilambrou discloses a method for detecting variations, comprising:

controlling count gate control by a first circuit to select a first oscillator (fig. 2, by mux; sec. 2);

generating a clock by the first oscillator in a second circuit (fig. 2, by RO1; sec. 2, ring oscillators in a second circuit);

counting the clock generated by the first oscillator by a third circuit (fig. 2, count/shift register; sec. 2, counter);

outputting a count of the clock generated by the first oscillator by the third circuit (fig. 2, by count/shift register; sec. 2);

selecting a second oscillator in the second circuit (fig. 2, mux selects RO2);

generating a clock by the second oscillator in the second circuit (sec. 2);

counting the clock generated by the second oscillator by the third circuit (fig. 2, by count/shift register); and

outputting a count of the clock generated by the second oscillator by the third circuit (fig. 2, count/shift register outputs count out).

As per claim 22, Hatzilambrou discloses a third oscillator for which corresponding steps may be taken (fig. 2, RO3).

As per claim 23, Hatzilambrou discloses an apparatus to detect process variations comprising:

a first circuit to control count gate control (fig. 2, mux; sec. 2);

a first oscillator to generate a clock, wherein the first circuit is to select the clock generated by the first oscillator (fig. 2, ring oscillator RO1; sec. 2);

a second circuit to count the clock generated by the first oscillator and to output the count of the clock generated by the first oscillator (fig. 2, count/shift register; sec. 2, counter); and

a second oscillator to generate a clock, wherein the first circuit is to select the clock generated by the second oscillator, and the second circuit is to count the clock generated by the second oscillator and is to output the count of the clock generated by the third oscillator (fig. 2, RO2; sec. 2).

As per claim 24, Hatzilambrou discloses a third oscillator for which corresponding steps may be taken (fig. 2, RO3).

As per claim 26, Hatzilambrou discloses a standard ring oscillator (sec. 2).

As per claim 29, Hatzilambrou discloses a multiplexer (sec. 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-9, 11-20, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hatzilambrou as applied to claims 1, 10 and 24 above, and further in view of IEEE Std 1149.1-1990, "IEEE Standard Test Access Port and Boundary-Scan Architecture", (includes IEEE Std 1149.1a-1993), 1993 ("IEEE").

As per claim 8, while Hatzilambrou teaches testing a chip with standard testing equipment (sec. 2), Hatzilambrou is silent with respect to a JTAG interface. IEEE teaches an interface standard that is commonly referred to as JTAG (page iii). At the time of the invention, it would have been obvious to one skilled in the art to apply IEEE's standard to interface with Hatzilambrou's testing equipment, since IEEE's standard is a well-known standard for test access ports.

As per claim 2, IEEE teaches the controlling comprises: activating a scan signal (sec. 3.4, TDI); toggling a clock signal (sec. 3.2, TCLK); and setting a reset signal on (sec. 5.3, TRST).

As per claim 3, IEEE teaches controlling further comprises the steps of: selecting an oscillator by activating and toggling the signals; enabling the oscillator; and setting the reset signal off (sec. 5.3, 8.1 & 10.2).

As per claim 4, IEEE teaches the controlling further comprises the step of toggling the clock signal for a period of time (sec. 3.2).

As per claim 5, Hatzilambrou teaches the step of generating further comprises the steps of: outputting the count into a counter (fig. 2). IEEE teaches reading data into a scan chain (sec. 8.2 & 8.3).

As per claim 6, Hatzilambrou teaches toggling further comprises the step of storing the output of the toggle in a counter (sec. 2).

As per claim 7, IEEE teaches the step of toggling a clock for reading out the clock count (sec. 8.1 & 10.2).

As per claim 9, IEEE teaches communicating with a JTAG interface (page iii).

As per claim 11, IEEE teaches the first circuit comprises: a scan signal; and a clock signal, wherein the scan signal and the clock signal turn on at least one clock (sec. 3.2, 3.4 & 8.1).

As per claim 12, IEEE teaches the first circuit further comprises: a reset signal; and an enable signal, wherein the enable signal enables the at least one clock (sec. 5.3 & 8.1).

As per claim 13, IEEE teaches the clock signal is toggled for a period of time (sec. 3.2).

As per claim 14, Hatzilambrou teaches the second circuit further comprises outputting a count of the toggle (sec. 2).

As per claim 15, Hatzilambrou teaches the third circuit comprises a counter (fig. 2). IEEE teaches a scan chain for data (sec. 8.2 & 8.3).

As per claim 16, Hatzilambrou teaches the at least one count is input to the counter (sec. 2).

As per claim 17, IEEE teaches the reset signal is input to the counter (sec. 5.3).

As per claim 18, IEEE teaches the scan chain further comprises a read signal, wherein the read signal reads the count into the scan chain (sec. 8.1 & 10.2).

As per claim 19, IEEE teaches the clock signal is toggled to read out the count from the scan chain (sec. 8.1 & 10.2).

As per claim 20, IEEE teaches the scan chain communicates with a JTAG interface (page iii).

As per claims 27 and 28, LTRAN and RTRAN are well known process parameters.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 571-272-3669. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

aw
March 23, 2005

THOMAS LEE
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